Remarks

The above Amendments and these Remarks are in reply to the final Office action mailed February 8, 2007.

I. Status of the Claims

Currently, claims 2-16, 18-20, 27-28, and 30-57 are pending. Claims 45-56 are withdrawn from consideration. Claim 6 was objected to under 37 CFR 1.75(c) as failing to further limit the subject matter of the previous claim. Claims 33 and 34 were rejected under 35 USC 112, second paragraph, as being indefinite. Claims 6, 15-16, 18-20, and 57 were rejected under 35 USC 102(e) as being anticipated by Chen, US Patent Publication 20030062594. Claims 2-5, 7-14, 27, 28, 30-32, and 35-44 were rejected under 35 USC 103(a) as being unpatentable over Chen.

II. Discussion of Claim Amendments

As discussed in following sections, claims 6, 33, and 34 were reworded to address the Examiner's concerns regarding clarity. Claim 18 was amended to depend from claim 16, rather than cancelled claim 17, from which it formerly depended. None of these changes constitutes new matter.

III. Claim Objection: Claim 6

Claim 6 was objected to as failing to further limit the subject matter of a previous claim. Claim 6 depends from claim 2, which depends from claim 57.

Applicant argued, in the response of Nov. 21, 2006, that claim 6 did in fact limit the subject matter of claim 57, from which it depended, and Applicant continues to believe this to be the case. To further prosecution, however, Applicant has amended claim 6 to explicitly recite that the semiconductor or conductive layer of the prior claim is not a semiconductor layer.

IV. 35 USC 112 Rejection: Claims 33 and 34

Claims 33 and 34 were rejected under 35 USC 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention.

Claim 33 formerly recited the semiconductor device of claim 27 wherein, for ***any*** portion of the conductive layer more than about 20 angstroms thick, the density of the titanium nitride is less than about 4.0 grams per cubic cm.

Claim 34 formerly recited the semiconductor device of claim 27 wherein, for ***any*** portion of the film more than about 20 angstroms thick, the resistivity of the titanium nitride is greater than about 300 microOhm-cms.

In rejecting these claims, the Examiner describes the phrase "for any portion" as precatory language. In an attempt at clarification, Applicant has amended these claims, replacing the word "any" with the word "a". Applicant does not intend or believe this amendment to be a change in scope, but hopes this formulation will prove more acceptable to the Examiner.

V. 35 USC 102 Rejection: Claims 57, 6, 15-16 and 18-20

Claims 57, 6, 15-16 and 18-20 were rejected under 35 USC 102(e) over Chen. Claims 57, 6, 15-16, and 18-20 were rejected under 35 USC 102(e) over Chen.

Claim 57 recites a semiconductor device comprising: a silicide layer; a grown dielectric antifuse layer on and in contact with the silicide layer; and a conductive layer or semiconductor layer on and in contact with the grown dielectric antifuse layer, wherein the silicide layer and the grown dielectric antifuse layer are portions of the semiconductor device, and wherein the grown dielectric antifuse layer has suffered dielectric breakdown, such that an electrical connection exists between the silicide layer and the conductive layer or semiconductor layer.

The Examiner finds a silicide layer in layer 56 of Figs. 8 and 9 of Chen. Paragraph [0026] of Chen describes this layer as "a doped polysilicon layer, a doped amorphous silicon layer or a silicide layer."

The Examiner further considers the stack 60, shown in Fig. 9, to be "a grown dielectric antifuse layer". Dielectric stack 60, in this figure, includes bottom oxide layer 57, silicon nitride layer 58, and top oxide layer 59. The Examiner considers the conductive layer or semiconductor

layer of claim 57 to be layer 66, for example of Figs. 10 and 11. Layer 66 is a metal conductive layer, as in paragraph [0028].

Applicant will concede that layer 56 may, in one embodiment, be silicide. Applicant will further concede that the dielectric rupture antifuse of Chen, which is a stack of three dielectric materials, may include a grown dielectric layer. But Applicant will show that Chen does not teach the combination of a) a silicide layer, b) a grown dielectric antifuse layer on and in contact with the silicide layer, and c) a semiconductor or conductive layer on and in contact with the grown dielectric antifuse layer.

Recall that claim 57 recites a silicide layer, a grown dielectric antifuse layer *on and in contact with* the silicide layer, and a conductive or semiconductor layer *on and in contact with* the grown dielectric antifuse layer. For Chen to anticipate this claim, then, a dielectric antifuse layer must be identified which has three characteristics: a) it is grown, b) it is in contact with a silicide, and c) it is in contact with a conductive or semiconductor layer. Applicant will show that none of layers 57, 58, 59, or stack 60, satisfies all three conditions.

In paragraph [0027], Chen teaches formation of the preferred embodiment, including three layers, a bottom oxide layer 57, a silicon nitride layer 58, and a top oxide layer 59. The bottom oxide layer 57 is described this way:

> To form the ONO dielectric layer 60, a ***native oxide*** layer with a thickness of 10-50 angstroms is first formed on the surface of the silicon conductive layer 56 and functions as the bottom oxide layer 57. (emphasis added)

This layer may be thermally grown, and is part of dielectric antifuse 60, a three-layer stack. But, in the passage above, layer 57 is described by Chen as a native oxide, which is formed *on the surface* of silicon conductive layer 56. The term "native oxide" is conventionally used to describe the oxide formed of a metal, semiconductor, or alloy such as silicon (silicon dioxide, SiO_2), aluminum (alumina, Al_2O_3), or an alloy of these materials. An oxide grown on a silicide is not conventionally described by the term "native oxide". Thus, in describing layer 57 as a native oxide, one skilled in the art would assume that this layer is grown on a silicon layer, not on a silicide layer. If layer 57 is a *grown* native oxide, it is not in contact with a silicide. The Examiner may suggest that paragraph [0026] teaches that layer 56 may be a silicide layer rather than a silicon layer, and thus that layer 57 may have been grown on silicide layer 56. Applicant believes this cannot be inferred, however. It is not conventional to grow an oxide layer on a silicide layer, and Chen gives

no teaching of how to do so. If a silicide layer were to be used as layer 56, the skilled artisan would assume that the bottom oxide layer in contact with this silicide layer was deposited rather than grown. Applicant believes one skilled in the art would interpret layer 56 to be either grown on silicon or deposited on a silicide. In short, this layer is *either* grown *or* in contact with a silicide, but not both. There is no specific teaching in Chen of a grown dielectric antifuse layer on and in contact with a silicide layer.

Further, recall that there is a third requirement for this layer: It must also be in contact with a semiconductor or conductive layer. It is entirely clear that layer 57 is not in contact with a conductive or semiconductor layer, such as layer 66 in Chen.

The next layer in the antifuse stack 60 is silicon nitride layer 58. In paragraph [0027], Chen is clear that this layer is deposited, not grown; thus this layer cannot be considered a grown dielectric antifuse layer. Further, this layer is in contact with *neither* a silicide layer *nor* a conductive or semiconductor layer.

The third layer 59 is an oxide or oxynitride layer which is formed by oxidizing silicon nitride layer 58. This is arguably a grown dielectric antifuse layer, and is in contact with conductive layer 66 above it. But the claim calls for the grown dielectric antifuse layer to be on and in contact with a *silicide* layer. Third layer 59 clearly is on and in contact with silicon nitride layer 58, not with a silicide, as in the claim.

Dielectric stack 60 is an antifuse, and is in contact with both a silicide (56, in some embodiments) and a conductive layer 66. But the claim recites that the dielectric antifuse layer must be *grown*. Dielectric stack 60 cannot be described as a grown dielectric antifuse layer, since its largest thickness, silicon nitride layer 58, is deposited rather than grown. None of layers 57, 58, 59, or 60 has all of the characteristics of the dielectric antifuse layer of the claim.

The embodiment of Chen described in paragraphs [0026] through [0028], then, does not teach the specific combination recited in claim 57: a silicide layer, a grown dielectric antifuse layer on and in contact with the silicide layer, and a conductive or semiconductor layer on and in contact with the grown dielectric antifuse layer.

Toward the end of paragraph [0027], Chen states:

> However, the dielectric layer 60 is not limited to the ONO dielectric layer only, and other dielectric layer such as a single dielectric layer or a stacked dielectric layer composed of at least two dielectric materials are also applicable in the present invention.

Chen arguably teaches here that layer 60 may be a single layer, rather than the three-layer stack described in paragraphs [0026] and [0027], and pictured in Figs. 9 through 11. But Applicants can find no teaching in Chen that this single layer is a grown dielectric layer on and in contact with a silicide layer. As Applicant has explained, it is not conventional to grow a high-quality dielectric layer (as required for an antifuse) on a silicide layer. The only teaching of which Applicant is aware that suggests growing a dielectric layer on a silicide for use as a dielectric rupture antifuse appears in the teachings of the present invention, and use of this suggestion would be impermissible hindsight. Without specific teaching of a dielectric layer grown on a silicide layer, one skilled in the art would assume that a single-layer dielectric antifuse in Chen was either a) a silicon dioxide layer thermally grown on silicon, or b) a dielectric layer deposited on a silicide.

Claim 16 depends from claim 57, 6, and 15, and includes the limitations that the conductive or semiconductor layer is not a semiconductor layer (claim 6), that the conductive layer comprises a metal (claim 15), and that the conductive layer forms a portion of a Schottky diode.

A Schottky diode is formed when semiconductor material, typically intrinsic or lightly doped n-type silicon, is electrically in contact with a conductor, such as a metal or silicide, forming a rectifying junction. Applicant can identify no teaching in Chen showing that conductive layer 66, which the Examiner has identified as this conductive layer, is in electrical contact with a semiconductor material. There is no semiconductor layer disclosed *above* layer 66. After rupture of dielectric stack 60, metal conductive layer 66 is in electrical contact with layer 56 (paragraph [0028]). The Examiner has interpreted layer 56 as a silicide layer, not a silicon layer. A junction between silicide layer 56 and metal layer 66 will not form a Schottky diode; one of the layers must be a semiconductor in order to form a Schottky diode. In embodiments of Chen, layer 56 is silicon, rather than a silicide, but claim 57, from which this claim depends, requires a silicide layer in contact with a grown dielectric antifuse layer; if layer 56 is silicon, rather than silicide, this is another way in which these claims distinguish over Chen.

In contrast, and by way of illustration, Fig. 5 of the present application, described in paragraphs [0064]-[0067] of the present application, shows a Schottky diode formed between conductive layer 204 and lightly doped n-type or intrinsic layer 206.

Applicant has shown that Chen does not teach or suggest the limitations of claim 57, and requests that the 35 USC 102(e) rejections of claim 57, and of its dependent claims 6, 15, 16 and 18-20, be withdrawn.

VI. <u>35 USC 103 Rejections over Chen: Claims 2-5, 7-14, 27, 28, 30-32, and 35-44</u>

Claims 2-5, 7-14, 27, 28, 30-32, and 35-44 were rejected under 35 USC 103(a) as being unpatentable over Chen. All of the claims included in this section depend from claim 57. In Section V of these remarks, Applicant explained that Chen does not teach the limitations of claim 57, and thus Applicant respectfully maintains that these claims also distinguish over the teachings of Chen.

Additionally, regarding the rejection of claim 9, the Examiner says:

> In re claim 9, Chen discloses the device of claim 2, but does not expressly disclose the conductor layer being a semiconductor layer. However, semiconductor layers are well known in the art to be used as conductor layers and it would have been obvious for one skilled in the art at the time of the invention to use a semiconductor layer as the top conductor, for the purpose, for example, of less process steps in switching from semiconductor to metal fabrication.

Applicant will point out, however, that claim 9 recites the semiconductor device of claim 2 wherein the conductor or semiconductor layer on and in contact with the grown dielectric antifuse layer is ***a lightly doped or intrinsic semiconductor layer***.

The Examiner will be aware that it is conventional in some devices to dope silicon (or other semiconductor materials) with conductivity-enhancing dopants such as boron (a P-type dopant) or phosphorus (an N-type dopant). The Examiner is correct that it is well-known to use a *heavily doped* semiconductor material as a conductor. Chen specifies in paragraph [0026] that silicon layer 56, which is intended to be conductive, is doped. When a semiconductor material is intended to serve as a conductor, it will be heavily doped.

Claim 9, however, specifies that the layer on and in contact with the grown dielectric antifuse layer is *lightly doped or intrinsic* (undoped). Such a layer serves an entirely different electrical purpose. If a dielectric rupture antifuse separates a silicide layer from a heavily doped semiconductor layer, the contact made between these two layers when the antifuse is ruptured will be substantially *ohmic*, conducting current symmetrically in either direction. In contrast, if a dielectric rupture antifuse separates a silicide layer from a lightly doped or intrinsic semiconductor layer, the contact made between these layers when the antifuse is ruptured will be *rectifying*, forming a Schottky diode. Such a structure conducts current more readily in one direction than the other.

If one skilled in the art wished to replace the metal of Chen's conductor 66 with semiconductor material, it would be with *heavily doped* semiconductor material, which would cause the layer to have similarly conductive behavior. One skilled in the art would not replace a conductor with lightly doped or intrinsic semiconductor material, as the electrical behavior of the resulting device would be entirely different.

Claims 10, 11, and 12 all specify formation of, or the presence of, a Schottky diode, which will necessarily include a *lightly doped or intrinsic* semiconductor layer. As described, such a layer is not taught or suggested by Chen, and one skilled in the art would not replace a conductive layer with a lightly doped or intrinsic semiconductor layer.

Claims 28 and 30 both include the limitations that the conductive layer is titanium nitride, and that the conductive layer forms a portion of a Schottky diode. The Examiner asserts that Chen teaches this Schottky diode, but does not identify any such teaching. Applicant can find no Schottky diode, and indeed can find no diode of any sort, taught or suggested by Chen. Claims 36-44 also include such a Schottky diode limitation, and thus also distinguish.

In the Response to Argument in the Office action of February 8, 2007, the Examiner says:

> … examiner does not assert that the semiconductor layer of Chen is "heavily" doped, such language is inserted by applicant.

Applicant will readily concede that the Examiner did not assert that the semiconductor layer of Chen is heavily doped, and that "heavily doped" is indeed Applicant's language. But Applicant reiterates that *if* one skilled in the art were to replace a metal conductive layer with silicon, intending that silicon to serve the same purpose as the metal it replaces, and for the device to have the same operation after the suggested modification, that skilled artisan would employ *heavily doped* silicon. Lightly doped silicon, or intrinsic silicon, do not have the same conduction characteristics as heavily doped silicon, and would not be a suitable replacement.

The Examiner continues:

> Secondly, applicant does not address the merits of the rejection. Examiner cited in the Non-Final rejection mailed 8/22/06 a valid reason why one skilled in the art at the time of the invention would be motivated to use lightly doped or intrinsic silicon for the conductive layer. Such a use would simplify the process steps, allowing the device to be made cheaper and faster. And, contrary to applicant's assertion, lightly-doped or intrinsically doped silicon is still "doped" and is still conductive.

Applicant has returned to the rejection of August 22, 2006, and assumes the Examiner to be referring to the rejection of claim 9 on page 6 of that Office action, specifically the following passage:

> … semiconductor layers are well known in the art to be used as conductor layers and it would have been obvious for one skilled in the art at the time of the invention to use a semiconductor layer as the top conductor, for the purpose, ***for example of less process steps in switching from semiconductor to metal fabrication***. (emphasis added)

Applicant understands the Examiner to be suggesting that fabrication would have been simplified had metal layer 66 of Chen been a doped silicon layer rather than a metal layer, because this would avoid a switch from semiconductor to metal fabrication.

Applicant reiterates that the Examiner is interpreting the structure of Chen to be a silicide layer 56, a dielectric stack 60, and a conductive layer 66. The conventional way to form a silicide is to deposit a silicide-forming metal, such as titanium or cobalt, for example by a sputtering process, onto a silicon layer. Next these layers are annealed to react the silicide-forming metal with the silicon, forming the silicide. A wet etch typically follows to remove unreacted metal. Continuing to form the structure of Chen, the layers making up the dielectric stack 60 are formed, presumably by a combination of deposition and growth methods.

At this point, the next step is fabrication of the conductive layer 66. Applicant points out that semiconductor fabrication has already been interrupted at this point; i.e. the wafer is no longer in a silicon deposition chamber, and a metal deposition step has already taken place, as a necessary step to form the silicide layer 56. (Applicant is aware that in most embodiments of Chen, layer 56 is in fact silicon, not a silicide, but as those embodiments clearly cannot anticipate claim 57, Applicant will not address them.) Since semiconductor processing has already been interrupted, it is in no way clear to the Applicant that it would be simpler for the next layer to be doped silicon rather than a metal. Deposited doped silicon must either be doped in situ, requiring flow of at least a dopant gas as well as a precursor gas to form silicon, or must be doped following deposition by an ion implantation step. It not clear to Applicant that deposition of a metal is inherently more complex, at this point, than formation of a doped silicon layer. If Applicant has misinterpreted the Examiner's suggested motivation, Applicant invites the Examiner to clarify this point.

Finally, regarding the Examiner's assertion that lightly doped or intrinsically doped silicon is still doped, Applicant will respectfully point out that intrinsic silicon is in fact undoped silicon, with no dopant provided.

Applicant has shown that Chen does not teach or suggest the elements of claims 2-5, 7-14, 27, 28, 30-32, and 35-44 and respectfully requests reconsideration.

IV. Conclusion

Based on the above amendments and these remarks, reconsideration of claims 2-16, 18-20, 27-28, 30-44, and 57 is respectfully requested.

The Examiner's attention to this matter is greatly appreciated. **Should further questions remain, the Examiner is encouraged to contact the undersigned attorney by telephone.**

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

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